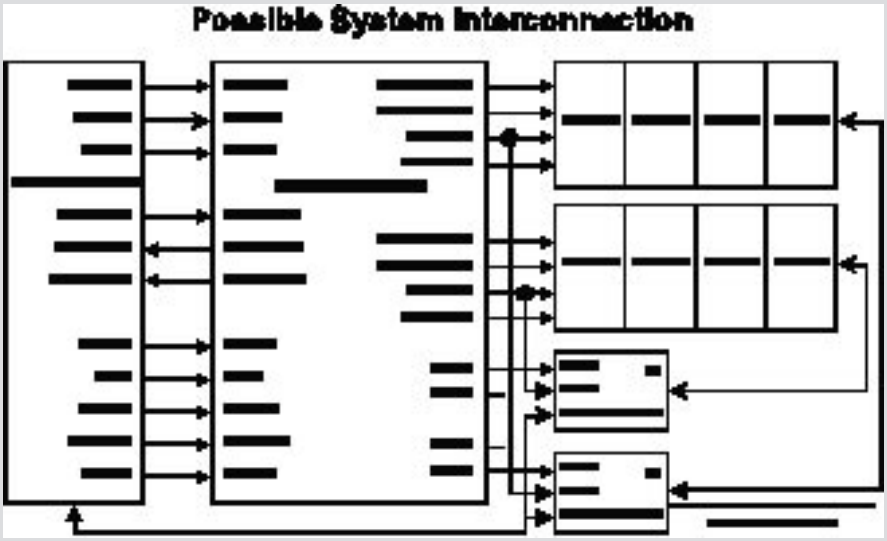
NSBMC096 Burst Memory Controller

- Interfaces Directly to the i960® CA Processor
- Integrated Page Cache Management
- Manages Page Mode Dynamic Memory Devices
- On-Chip Memory Address Multiplexer/Drivers
- Supports DRAMs From 256 Kbytes to 64 Mbytes
- 24-Bit Counter/Timer
- Non-Interleaved or Two-Way Interleaved Operation
- 5-Bit Bus Watch Timer
- Software-Configured Operational Parameters
- High-Speed/Low Power CMOS Technology



The NSBMC096 Burst Memory Controller is an integrated circuit that implements all aspects of DRAM control for high-performance systems using an i960 CA/CF Superscalar embedded processor. The NSBMC096 is functionally equivalent to the V96BMC.

The extremely high instruction rate achieved by these processors places extraordinary demands on memory system design if maximum throughput is to be sustained and costs minimized. Static RAM offers a simple solution for high-speed memory systems. However, high cost and low density make this an expensive and space consumptive choice.

Dynamic RAMs are an attractive alternative with higher density and low cost. Their drawbacks are slower access time and more complex control circuitry required to operate them. The access time problem is solved if DRAMs are used in page mode. In this mode, access times rival that of static RAM. The control circuit problem is resolved by the NSBMC096.

The function that the NSBMC096 performs is to optimally translate the burst access protocol of the i960 CA/CF Processor to the page mode access protocol supported by dynamic RAMs. The device manages one- or two-way interleaved arrangements of DRAMs such that during burst access, data can be read or written at the rate of one word per system clock cycle.

The NSBMC096 has been designed to allow maximum flexibility in its application. The full range of processor speeds is supported for a wide range of DRAM speeds, sizes and organizations.

No glue logic is required because the bus interface is customized to the i960 CA/CF Processor. System integration is further enhanced by providing a 24-bit heartbeat timer and a bus watch timer on-chip.

The NSBMC096 is packaged as a 132-pin PQFP with a footprint of only 1.3 square inches. It reduces design complexity and space requirements and is fully derated for

PROCESSORS SUPPORTED:
i960 CA/CF Processors

AVAILABILITY:
Fully available in 16, 25 and 33 MHz versions.

CONTACT:
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For international contacts see Appendix B.

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